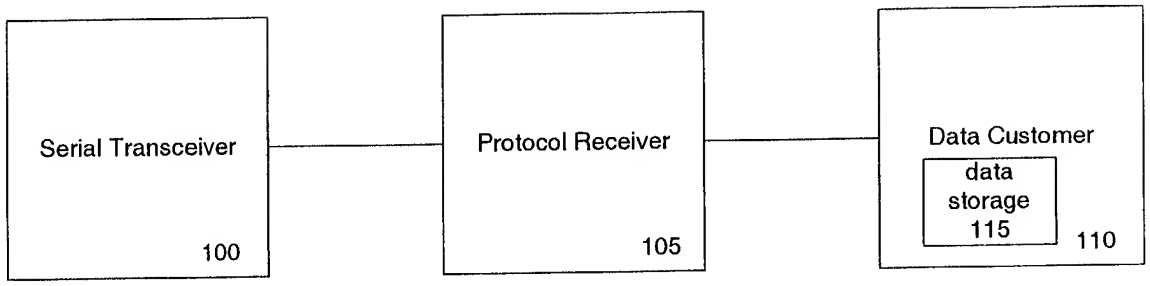
Serial Transceiver
100
Protocol Receiver
105
Data Customer
data storage
115
110

FIG. 1

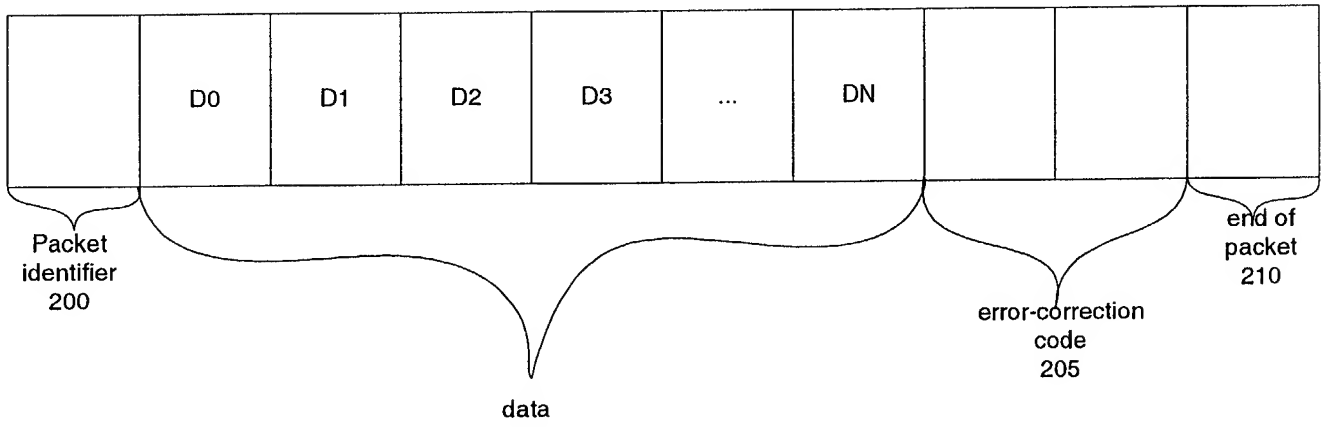
D0
D1
D2
D3
...
DN
Packet identifier 200
data
error-correction code 205
end of packet 210

FIG. 2

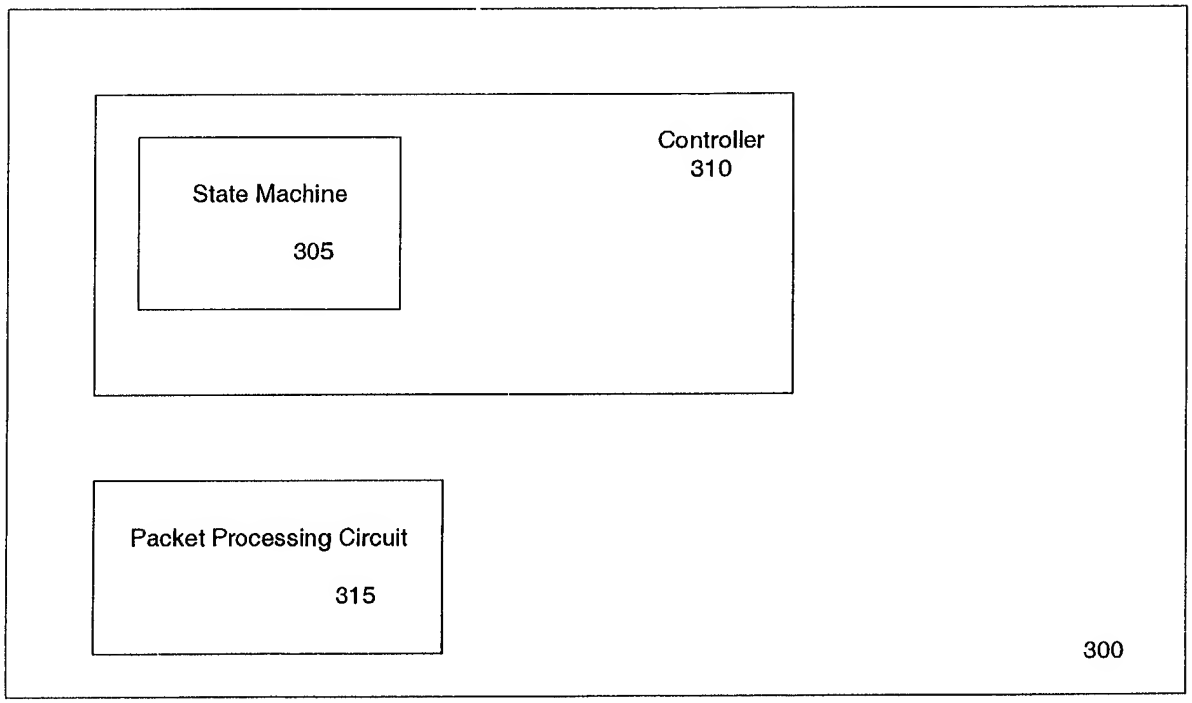
Controller
310
State Machine
305
Packet Processing Circuit
315
300

FIG. 3

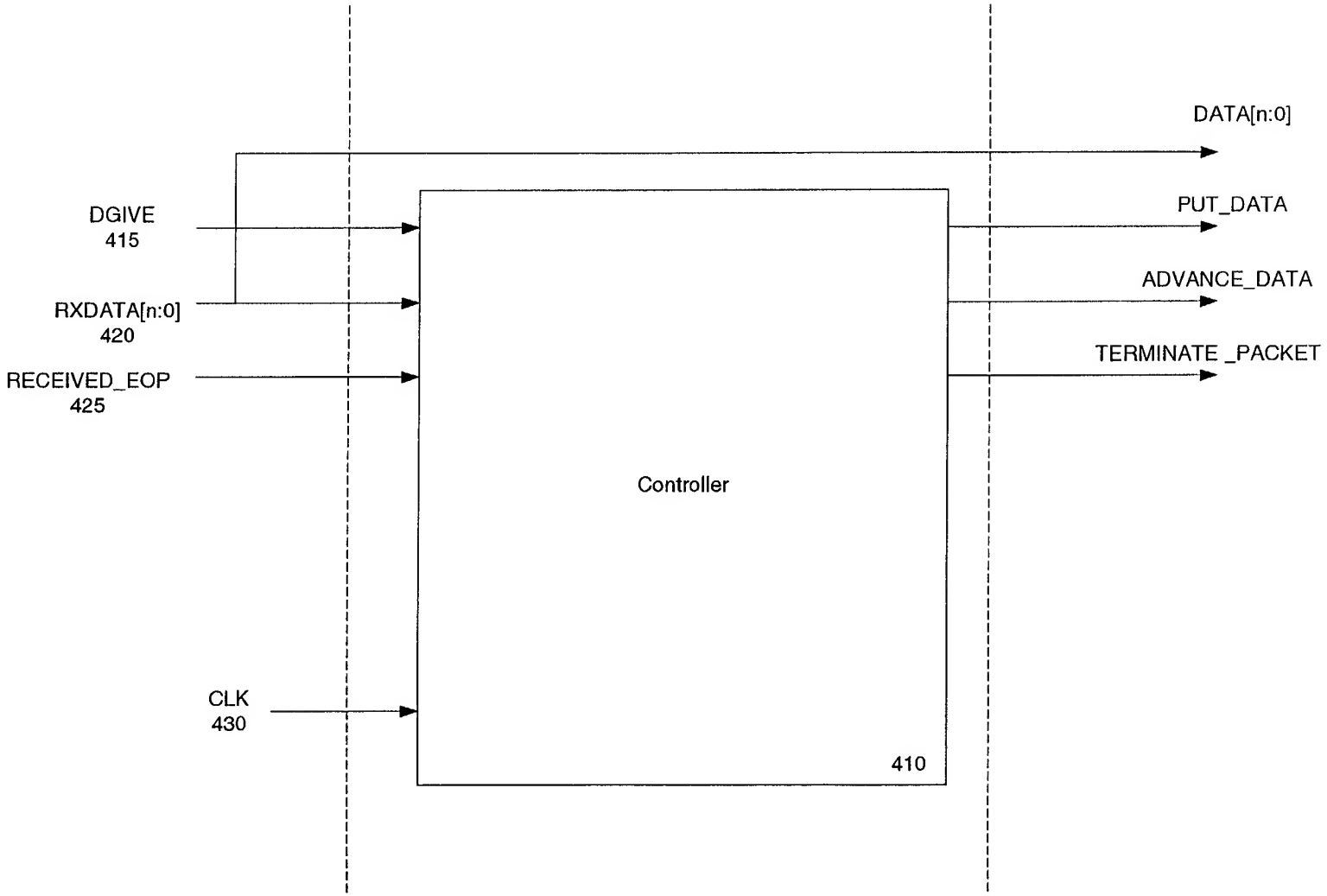
DATA[n:0]
DGIVE
415
PUT_DATA
RXDATA[n:0]
420
ADVANCE_DATA
RECEIVED_EOP
425
TERMINATE _PACKET
Controller
CLK
430
410

FIG. 4

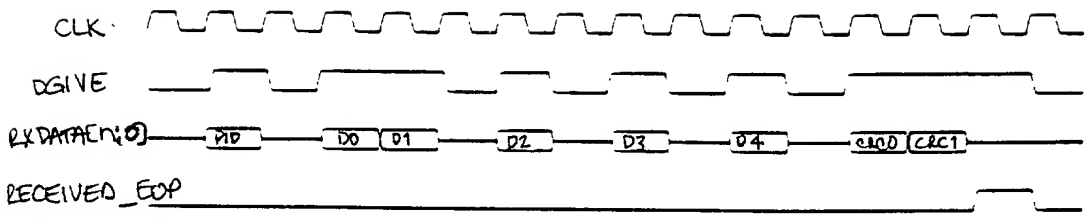

FIG. 5

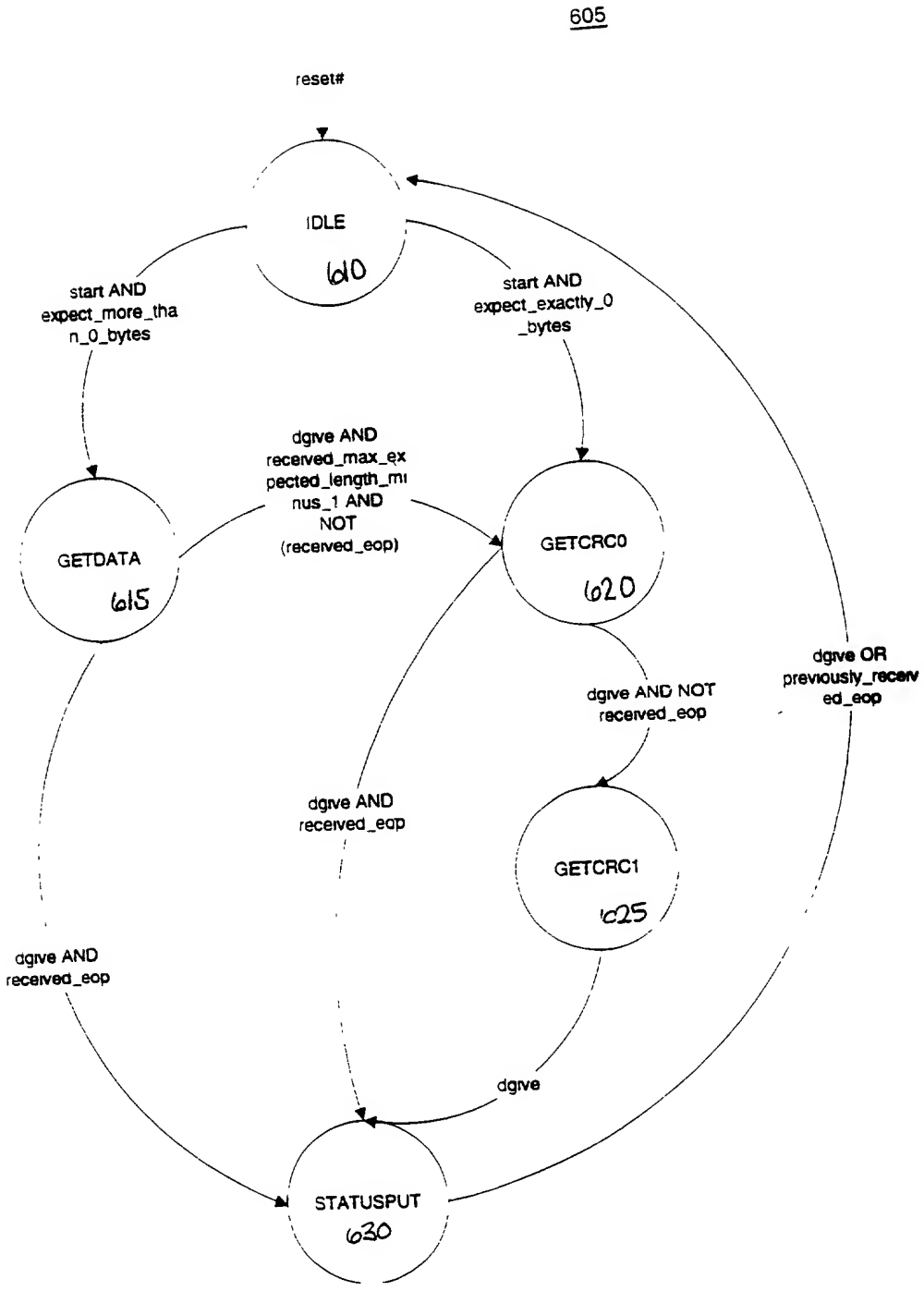
605
reset#
IDLE
610
start AND expect_more_than_0_bytes
start AND expect_exactly_0_bytes
GETDATA
615
dgrve AND received_max_expected_length_minus_1 AND NOT (received_eop)
GETCRC0
620
dgrve OR previously_received_eop
dgrve AND NOT received_eop
dgrve AND received_eop
GETCRC1
625
dgrve AND received_eop
dgrve
STATUSPUT
630

FIG. 6

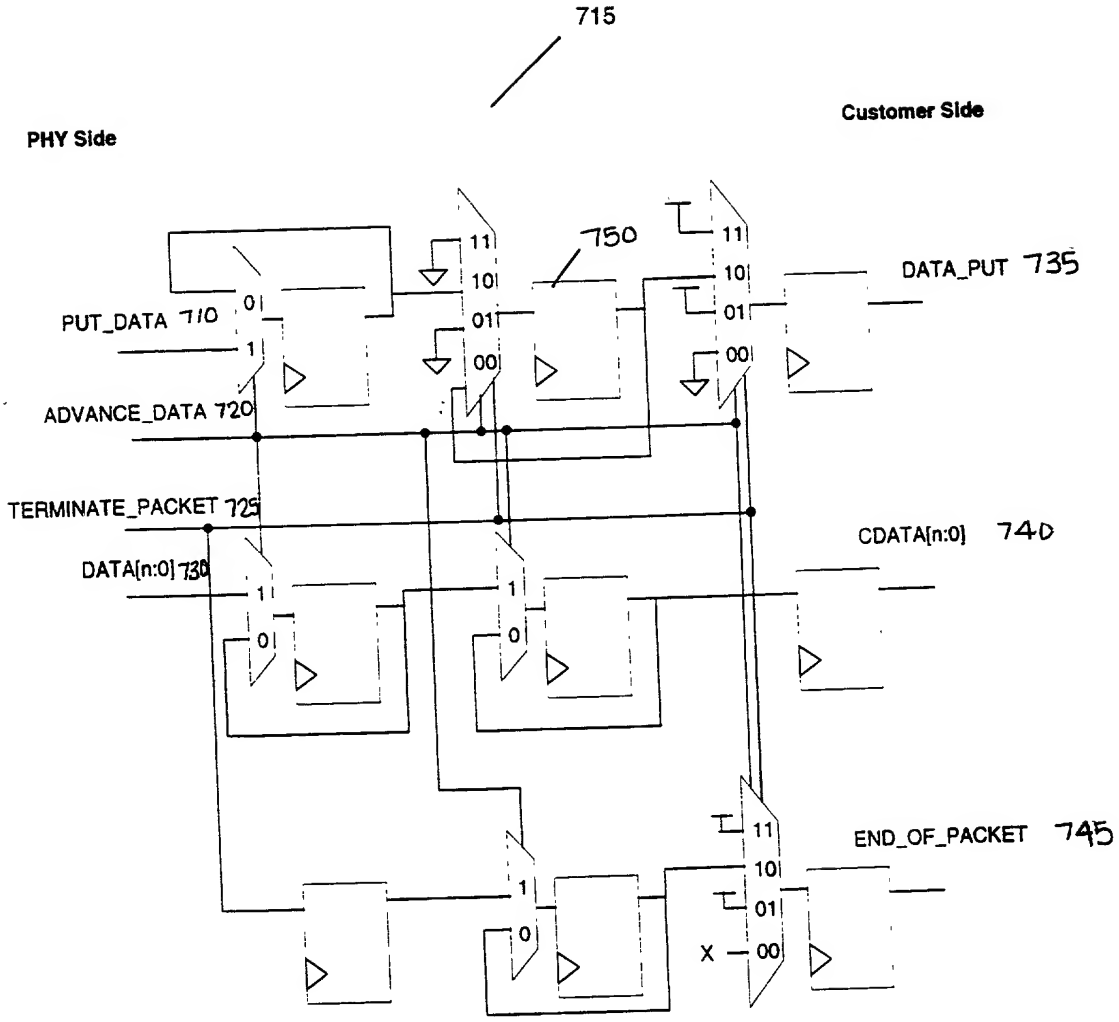
715
PHY Side
Customer Side
750
PUT_DATA 710
ADVANCE_DATA 720
TERMINATE_PACKET 725
DATA[n:0] 730
DATA_PUT 735
CDATA[n:0] 740
END_OF_PACKET 745
11
10
01
00
0
1
X

FIG. 7

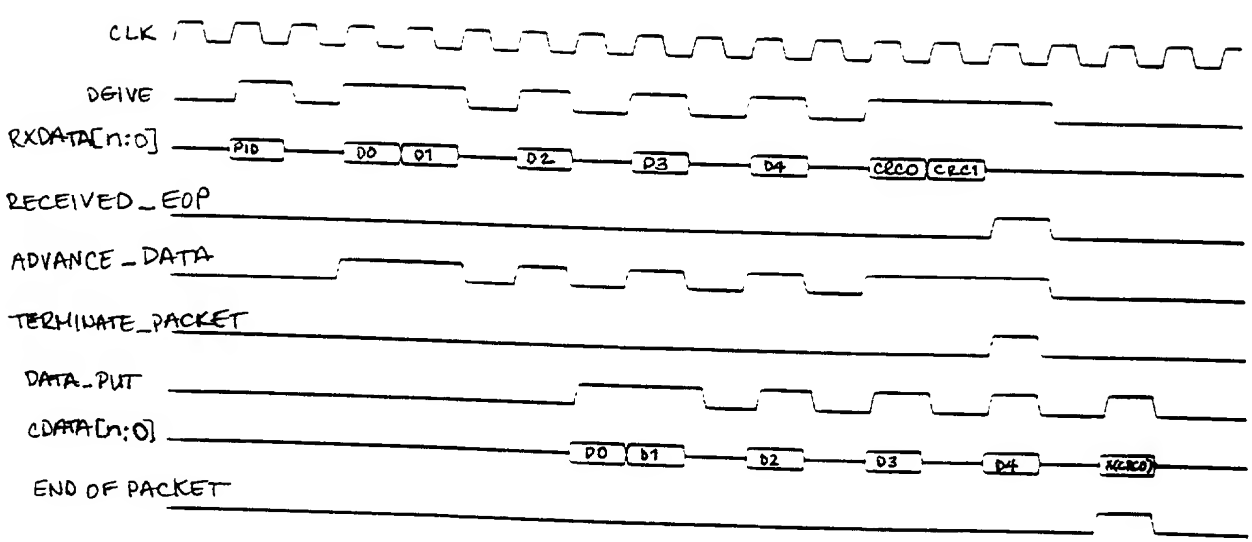
CLK
DGIVE
RXDATA[n:0]
PID
D0
D1
D2
D3
D4
CRC0
CRC1
RECEIVED_EOP
ADVANCE_DATA
TERMINATE_PACKET
DATA_PUT
CDATA[n:0]
D0
D1
D2
D3
D4
END OF PACKET

FIG. 8